

REPORT DOCUMENTATION PAGE				Form Approved OMB No. 0704-0188	
The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing the burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.					
PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.					
1. REPORT DATE (DD-MM-YYYY) 05/03/2005		2. REPORT TYPE Final Technical Report		3. DATES COVERED (From - To) 06/01/2003 - 12/31/2003	
4. TITLE AND SUBTITLE Development of Buffer Layer Technologies for LWIR and VLWIR HgCdTe Integration on Si				5a. CONTRACT NUMBER DAAD 19-03-1-0107	
				5b. GRANT NUMBER N/A	
				5c. PROGRAM ELEMENT NUMBER N/A	
				5d. PROJECT NUMBER N/A	
6. AUTHOR(S) Golding, Terry, D.				5e. TASK NUMBER N/A	
				5f. WORK UNIT NUMBER N/A	
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) University of North Texas Office of Sponsored Projects P.O. Box 305250 Denton, TX 76203-5250				8. PERFORMING ORGANIZATION REPORT NUMBER G73293	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) Army Research Office Attn: AMSRD-ARL-RO-SG-SI P.O. Box 12211 Research Triangle Park, NC 27709-2211				10. SPONSOR/MONITOR'S ACRONYM(S) ARO / ONR	
				11. SPONSOR/MONITOR'S REPORT NUMBER(S) 45408e1-EL	
12. DISTRIBUTION/AVAILABILITY STATEMENT Public Distribution / Availability Unlimited					
13. SUPPLEMENTARY NOTES N/A					
14. ABSTRACT Obedient Buffers A method of forming GexSi1-x films by thermal oxidation of Ge+-implanted Si was developed further. The process involves segregation of the implanted Ge during oxidation to form a distinct Ge-rich layer at the oxide interface. The composition of the segregated layer can be altered by varying the oxidation conditions as a result of the kinetic competition between oxidant interdiffusion of the segregated layer with the underlying Si substrate. Rutherford backscattering results show that the Ge becomes more dilute at higher oxidation temperatures. Below a critical thickness, the segregated film forms pseudomorphic growth on the underlying Si. However, the observed critical thickness greatly exceeds the value predicted for pseudomorphic growth. Dislocation-free relaxation of the GexSi1-x films formed within a Si-on-insulator (SOI) wafer is achieved with a unique vapor injection technique. The encapsulation of the segregated film by the oxide layers in the SOI ensures that the injected vapor remains within the volume of the film to relax the strain and are not lost to the underlying substrate.					
15. SUBJECT TERMS Development of Buffer Layer Technologies for LWIR and VLWIR HgCdTe Integration on Si					
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Dr. Terry D. Golding
U	U	U	UU	3	19b. TELEPHONE NUMBER (Include area code) (940) 565-3271

# FINAL PROGRESS REPORT

## Development of Buffer Layer Technologies for LWIR and VLWIR HgCdTe Integration on Si

DAAD 19-03-1-0107

To  
Army Research Office  
ATTN: AMSRD-ARL-RO-SG-SI  
P.O. Box 12211  
Research Triangle Park  
NC 27709-2211

### **Forward:**

This is a final report for Research agreement No. DAAD 19-03-1-0107, “Development of Buffer Layer Technologies for LWIR and VLWIR HgCdTe Integration on Si”. This was awarded 6/1/03 and was originally a 36 month program, but was cancelled due to lack of funds from MDA (Dr. Meimi Tidrow). This final report is appearing significantly later than typically required, due to some prospect that MDA would recover some funds for its continuation. The reports here thus are only for the six months of funding initially received.

### **Statement of Problem:**

This program proposed to develop and evaluate manufacturable, cost-effective buffer layer technologies that would allow either hybrid or monolithic integration of LWIR and VLWIR HgCdTe infrared focal plane arrays with standard Si-based integrated circuits.

Previous efforts have been thwarted by the large lattice mismatch (~19%) that prevents the growth of high-quality HgCdTe epilayers (with defect density  $< 5 \times 10^5/\text{cm}^2$ ) directly onto a Si wafer. Furthermore, molecular beam epitaxial growth (required for state-of-the-art HgCdTe films) can only be achieved on a Si(211)B surface orientation. Since Si-based digital electronics utilizes the (100) orientation exclusively, this limitation presents an almost insurmountable barrier to monolithic integration. Suitable buffer layer technologies that can compensate for the large lattice mismatch (and crystallographic orientation change) are urgently needed to overcome these problems.

Currently ZnTe/CdTe layers are used to buffer HgCdTe epilayers on Si wafers. This technology enables the growth of HgCdTe epilayers of high enough quality to allow fabrication of MWIR photodiode arrays with high performance. However, the template

quality of the resultant buffer layers (defect density and/or lattice matching with HgCdTe) is simply not adequate for the realization of LWIR and/or VLWIR HgCdTe, due to the increased sensitivity of the electro-optical properties of the HgCdTe to the defect density at these reduced bandgaps.

Three buffer layer technologies are proposed each of which avoids the typical inherent problems associated with 'alternative' buffer technologies, such as dopant diffusion into the active device region, and incompatibility with IR focal plane fabrication lines, and provides unique solutions to the issues preventing the realization of LWIR HgCdTe on Si.

.These technologies are based on i) the use of ultrathin, GeSi films as obedient buffers ii) wafer bonding of lattice-matched buffers.

### **Summary of the most important results:**

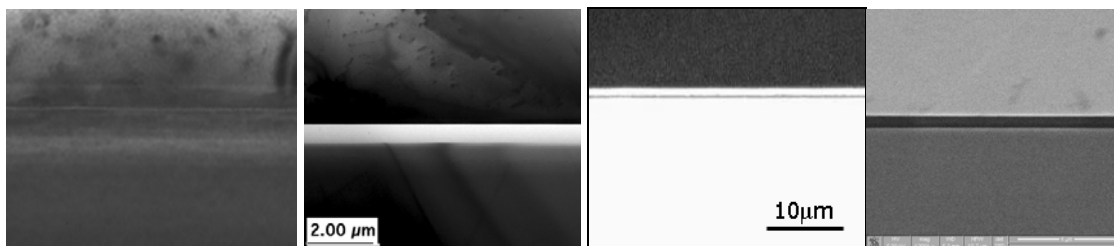
#### **Obedient Buffers**

A method of forming  $\text{Ge}_x\text{Si}_{1-x}$  films by thermal oxidation of  $\text{Ge}^+$ -implanted Si was developed further. The process involves the segregation of the implanted Ge during oxidation to form a distinct Ge-rich layer at the oxide interface. The composition of the segregated layer can be altered by varying the oxidation conditions as a result of the kinetic competition between oxidation and the interdiffusion of the segregated layer with the underlying Si substrate. Rutherford backscattering results show that the Ge-rich layer becomes more dilute at higher oxidation temperatures. Below a critical thickness, the segregated film forms pseudomorphically on the underlying Si. However, the observed critical thickness greatly exceeds the value predicted for pseudomorphic growth.

Dislocation-free relaxation of the  $\text{Ge}_x\text{Si}_{1-x}$  films formed within a Si-on-insulator (SOI) wafer is achieved with a unique vacancy-injection technique. The encapsulation of the segregated film by the oxide layers in the SOI ensures that the injected vacancies remain within the volume of the film to relax the strain and are not lost to the underlying substrate.

#### **Wafer Bonding**

Wafer bonding offers the ability to integrate dissimilar and orientationally differing layers on the substrate of choice. In particular, materials with large lattice misfits or different lattice structures across interfaces can be bonded without causing defect formation in the crystal adjacent to the bonded interfaces. Particularly important for this program is the ability to produce orientation tailored heterostructures, such as CdTe(211B)/Si(100).



**Fig. 1.** (a) Cross-sectional TEM image of the directly bonded CdTe(211)/Si(100). Scale bar = 50nm. Some voids were observed along the bonded interface due to high surface roughness of the CdZnTe(211) wafers. Low temperature integration of CdZnTe(211)/Si(100) by spin-on-glass (SOG) bonding layers resulted in well-bonded interface without voids, as shown in (b). (c) CdZnTe(211) thin layer transferred onto Si(100). (d) Low temperature integrated GaAs(100)/Si(100) with SOG bonding layers. Scale bar = 4 μm.

### **Listing of all publications:**

‘Monolithic Integration of HgCdTe with Si(100)’, T.D. Golding, O.W. Holland, J. H. Dinan, T. Almedea, M. Kim, W. Kirk, *Jour. of Elec. Mats.* **32**, 882 (2003).

‘Pseudomorphic and Relaxed GeSi:Si Heterostructures Formed By Ion Implantation for Heteroepitaxial Templates’, O. W. Holland, K. Hossain and T. D. Golding, M. F. Chisholm, 24<sup>th</sup> Army Science Conference Proceedings, Orlando, Florida Nov 29- Dec 2, (2004) NP-13, [www.asc2004.com/Manuscripts/sessionN/N.html](http://www.asc2004.com/Manuscripts/sessionN/N.html)

### **List of all participating scientific Personnel:**

Dr. Terry Golding (PI)  
Dr. Wayne Holland (PI)  
Dr. M. Kim (PI)

Mr. Khalid Hossain (Graduate student)  
Dr. Brian Gorman (Research Scientist)

### **Report of Inventions:**

None